Applicants respectfully submit that independent claim 1 is patentable over Jang because, for instance, Jang does not disclose or suggest forming a surface sensitive silicon oxide layer over the substrate. Nor does Jang teach or suggest forming a porous silicon oxide layer on the surface sensitive silicon oxide layer by thermal chemical vapor deposition, wherein the porous silicon oxide layer is deposited at a temperature of about 400°C or less.

The Examiner alleges that Jang discloses a surface sensitive oxide layer 12 in Table II. Applicants note that layer 12 is "a substrate layer" (col. 6, line 17), which is merely a dielectric layer. As defined at column 6, lines 45-56, the substrate layer 12 is "a microelectronics dielectric layer formed of silicon containing dielectric materials including but not limited to silicon oxide dielectric material, silicon nitride dielectric material and silicon oxynitride dielectric material, employing methods including but not limited to thermal oxidation methods, chemical vapor deposition (CVD) methods, physical vapor deposition (PVD) sputtering methods and reactive sputtering methods. Preferably, the microelectronics dielectric layer 12 is a silicon nitride dielectric layer formed employing chemical vapor deposition (CVD) methods." "Using the Kwok paper as a basis, a 'surface sensitive' silicon oxide layer in the context of the present invention, is interpreted to mean a silicon oxide underlayer having physical characteristics such that when a high ozone TEOS SACVD film as defined in the Kwok paper is deposited over the silicon oxide underlayer the wet etch rate (in a 6:1 BOE solution as understood by those of skill in the art) is greater than about 6000 Å/min." Specification at page 17, lines 13-18. Jang is devoid of any suggestion of a surface sensitive layer of the present invention.

The PECVD layer in sample 1 of Table II is **not** the substrate layer 12. As discussed at column 14, lines 35-46, the PECVD layer in sample 1 is "a conformal silicon oxide dielectric layer" formed after forming the silicon oxide layer and three-layer patterned conductor stack layers on the silicon semiconductor substrate "in accord with the schematic cross-sectional diagram of FIG. 4 and the methods employed in the description of the silicon semiconductor substrates produced for Example 1." Nor is the

PECVD layer in sample 1 a surface sensitive layer. Additionally, no porous silicon oxide layer is formed on the PECVD layer in sample 1.

Moreover, Jang **teaches away** from the invention as recited in claim 1 by specifying a substrate temperature of "about 440 to about 480 degrees centigrade" for the ozone assisted sub-atmospheric pressure thermal chemical vapor deposition (SACVD) of the silicon oxide dielectric layer 18 over the substrate layer 12 and conductor stack layers 17 (col. 7, lines 34-36). Claim 1 recites that the porous silicon oxide layer is deposited at a temperature of about 400°C or less.

Applicants further note that samples 2 and 3 shown in Table II of Jang include silicon oxide dielectric layers "formed **not** in accord with the general method of the . . . invention" as disclosed in Jang (col. 14, lines 54-55) (emphasis added). The examples involve forming silicon oxide dielectric layers at 400 degrees centigrade on silicon semiconductor substrates having silicon oxide substrate layers 12 and three-layer patterned conductor stack layers 42, 43, 44 formed thereon (col. 14, lines 35-40). Those silicon oxide layers formed on samples 2 and 3 were considered to produce undesirable results (col. 15, lines 33-41), and were not formed on surface sensitive silicon oxide layers.

For at least the foregoing reasons, Applicants believe claim 1 is patentable over Jang.

Claims 2-9 depend from claim 1, and are submitted to be patentable as being directed to additional features of the present invention as well as by being dependent from allowable claim 1. For example, claim 2 recites that the porous silicon oxide layer has a carbon content of at least 5 atomic percent. Claim 3 recites that the porous silicon oxide layer has a dielectric constant of between about 2.9 and 3.2. Although Jang mentions a dielectric constant of about 2.5 to about 3.3, Jang is referring to specific materials such as SOP, HSQ, FSQ, and SOG as listed in column 2, lines 3-20. The silicon oxide dielectric layer 18 in Jang is not formed from any of the materials listed in column 2, lines 3-20. Claim 7 recites forming a capping silicon oxide layer over the porous silicon oxide layer. Claim 9 recites that the surface sensitive and porous silicon

oxide layers are deposited in an in situ process. These features are completely absent from Jang.

Applicants respectfully assert that independent claim 10 is patentable over Jang because, for instance, Jang fails to teach or suggest depositing a plasma enhanced chemical vapor deposition (CVD) silicon oxide layer over the plurality of conductive lines from a plasma of tetraethyloxysilane (TEOS) and oxygen. Jang further fails to teach or suggest depositing a silicon oxide layer over the plasma enhanced CVD silicon oxide layer by a thermal CVD process from a gas mixture of a TEOS and ozone wherein the thermal silicon oxide layer has a dielectric constant of about 3.2 or less and a carbon content of at least about 5 atomic percent.

In Jang, the substrate layer 12 is formed prior to forming the conductor stacks, and thus does not constitute the PECVD silicon oxide layer formed over the plurality of conductive lines as recited in claim 10. The silicon oxide dielectric layer 18 which is formed over the conductor stacks is an SACVD layer (col. 7, lines 20-25), not a PECVD layer. As to the premetal dielectric layer (PMD) 40, it is not an intermetal dielectric film. The premetal dielectric layer 40 is formed prior to forming the conductor stacks 45. The Examiner further alleges that Jang discloses depositing a silicon oxide layer over the PECVD silicon oxide layer by a thermal CVD process from a gas mixture of TEOS and O_3 wherein the thermal silicon oxide layer has a dielectric constant of 3.2 or less and a carbon content of at least 5% at column 12, lines 55-61. Jang at column 12, lines 55-61, however, does not disclose the recited features as alleged by the Examiner. Indeed, Jang is devoid of any disclosure of carbon content in a thermal CVD silicon oxide layer.

Nothing in Jang suggests depositing a PECVD layer over the conductive lines and depositing a silicon oxide layer over the PECVD layer by a thermal CVD process from ozone and TEOS having the characteristics as recited in claim 10. For at least the foregoing reasons, claim 10 is patentable over Jang.

Claims 11-19 depend from claim 10, and are submitted to be patentable as being directed to additional features of the invention as well as by being dependent from

allowable claim 10. For example, claim 11 recites that the density of the thermal silicon oxide layer is less than or equal to about 1.7 g/cm^3. Claim 12 recites depositing a plasma enhanced CVD silicon oxide capping layer over the thermal silicon oxide layer. Claim 18 recites that the plasma enhanced and thermal CVD silicon oxide layers are deposited in an in situ process. These features are completely absent from Jang.

Claim 20

Apparatus claim 20 is withdrawn from consideration pursuant to the restriction requirement. Claim 20 recites a substrate processing system comprising a memory having a computer-readable program that encompasses any and every computer implementation of the process as recited in the process claims.

MPEP § 806.05(e) states: "In applications claiming inventions in different statutory categories, only one-way distinctiveness is generally needed to support a restriction requirement." Specifically, if it can be shown "(A) that the process *as claimed* can be practiced by another and materially different apparatus or by hand, or (B) that the apparatus *as claimed* can be used to practice another materially different process", then restriction is proper. *Id.* (emphasis in original). MPEP § 806.05(e) further states: "If applicant proves or provides convincing argument that there is no material difference . . . . , the burden is on the examiner to document another materially different process or apparatus or withdraw the requirement."

Applicants contend that the apparatus claim 20 is not materially distinct from the process claims (1-19) because the apparatus claims encompass any and every computer implementation of the process recited in the process claims, so that the apparatus claim is to be examined on the basis of the underlying process. In the present case, apparatus claim 20 defines the physical characteristics of a computer or computer component exclusively as functions or steps to be performed on or by a computer, and encompasses any and every product in the state class (e.g., computer, computer-readable memory) configured in any manner to perform that process. In addition, the specification does not include specific software, i.e., programming code recited to define the aforementioned functions. As a result, the apparatus claim 20 and process claims (1-19)

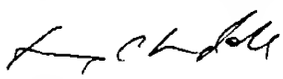
stand or fall together. Accordingly, Applicants respectfully request that the restriction requirement be withdrawn and that claim 20 be allowed.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claim 10 as follows.

10. (Amended) A **[process]** method for depositing an intermetal dielectric film over a plurality of conductive lines, the method comprising:

depositing a plasma enhanced chemical vapor deposition (CVD) silicon oxide layer over the plurality of conductive lines from a plasma of tetraethyloxysilane (TEOS) and oxygen; and

depositing a silicon oxide layer over the plasma enhanced CVD silicon oxide layer by a thermal CVD process from a gas mixture of a TEOS and ozone wherein said thermal silicon oxide layer has a dielectric constant of about 3.2 or less and a carbon content of at least about 5 atomic percent.